REMARKS

Claims 1-10 are presented for examination.

The drawings have been objected because they include reference characters not mentioned in the specification. In particular, the Examiner contends that characters c2, ca4 (FIG. 8B), ca12-ca15, ca20, c7 (FIGS. 9A-9B), da11 (FIG. 10B), da19-da20 (FIG. 11) and e4-e5, ea12-ea13 (FIGS. 12A-12C).

In response, the drawings have been corrected to delete these characters from the respective figures.

Claims 1, 2 and 6-10 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Per the Examiner's request, claims 1 and 6 have been amended to delete the word "said" before "layout pattern data" in lines 13 and 9, respectively. It is noted that the phrases "said layout pattern data" in claims 2 and 7 have the antecedent basis in claims 1 and 6, respectfully.

Also, per the Examiner's request, claims 8-10 have been amended to delete the word "said" before the phrase "extraction of the node."

In addition, claim 6 has been amended to correct an error.

Further, the Examiner takes the position that the phrase "a post layout simulation implementing part connected to said net list generation part for implementing a post layout simulation by using said net list" in claim 1 is not clear.

The Examiner's rejection is respectfully traversed. The pivotal issue generated by a rejection under the second paragraph of 35 U.S.C. § 112 is whether one having ordinary skill in the art, with the supporting specification in hand, would be able to ascertain the scope of the claims with reasonable precision. ***In re Moore***, 439 F.2d 1232, 169 USPQ 236 (CCPA 1971); ***In re Hammack***, 427 F.2d 1378, 166 USPQ 204 (CCPA 1970). It should be emphasized that

unpatented claims are reasonably construed in light of the supporting specification. ***In re Okuzawa***, 537 F.2d 545, 190 USPQ 464 (CCPA 1976); ***In re Royka***, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Moreover, reasonable precision is all that is required. See, for example, ***U.S. v. Telectronics Inc.***, 857 F.2d 778, 8 USPQ2d 1217; ***Hybritech, Inc, v. Monoclonal Antiobodies, Inc.***, 802 F.2d 1367, 231 USPQ 81 (Fed. Cir. 1986); ***In re Kroekel***, 504 F.2d 1143, 183 USPQ 610 (CCPA 1974).

A decision on whether a claim is invalid under this section of the statute requires a determination of whether those skilled in the art would understand what is claimed when the claim is read in light of the specification, ***Seattle Box Co. v Industrial Crating & Packing***, 731 F.2d 381, 385, 221 U.S.P.Q. 568, 574 (Fed. Cir. 1984). Claim language is viewed not in a vacuum, but in light of the teachings of the prior art and of the application disclosure as it would be interpreted by one possessing the ordinary level of skill in the art. ***In re Johnson***, 558 F.2d 1008, 194 USPQ 187 (CCPA 1977); ***In re Moore, supra***.

With the above legal precedents in mind, Applicants respectfully point out that the Examiner does not explain why one having ordinary skill in the art, armed with the supporting specification, would have been confused as to the scope of claim 1 when read in light of the disclosure. More specifically, it is not apparent why the phrase "a post layout simulation implementing part connected to said net list generation part for implementing a post layout simulation by using said net list" generates a ***prima facie*** basis to deny patentability to the invention defined in claim 1 under the second paragraph of 35 U.S.C. § 112 for indefiniteness.

It is respectfully submitted that the specification on page 7, lines 8-15, explains that "the post layout simulation is carried out by using the net list with parasitic elements..." Therefore, one skilled in the art would understand from the claim language that the post layout simulation

implementing part is connected to the net list generation part in order to implement a post layout simulation by using the net list.

It is believed that the claims, as now amended, fully comply with the statutory requirement to set out and circumscribe a subject matter area with a reasonable degree of precision and particularity.

Claims 1-10 have been rejected under 35 U.S.C. 102(e) as being anticipated by Ho. This rejection is respectfully traversed for the following reasons.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154.

Claim 1 recites a back annotation apparatus including:

-a pre-layout simulation implementing part for detecting nodes of which the potential changes when a predetermined signal is applied to a logic circuit;

-a layout pattern verification implementing part for implementing a predetermined layout pattern verification for layout patterns of said logical circuit;

-a parasitic element extraction part connected to said pre-layout simulation implementing part which extracts parasitic elements from said nodes of which the potential changes;

-a net list generation part connected to said parasitic element extraction part for generating a net list which includes all the devices included in said layout pattern data and parasitic elements extracted in said parasitic element extraction part; and

-a post layout simulation implementing part connected to said net list generation part for implementing a post layout simulation by using said net list.

Claim 6 recites the respective steps including:

-the step of detection of nodes of which the potential changes when a predetermined signal is applied to a logic circuit;

-the step of implementing a predetermined layout pattern verification with respect to a layout pattern of said logic circuit;

-the step of extracting parasitic elements from said nodes of which the potential changes;

-the step of generation of a net list including all the devices included in said layout pattern data and the parasitic elements extracted in said step of extracting parasitic elements; and

-the step of implementation of a post layout simulation by using said net list.

Considering the reference, Ho does not teach the pre-layout simulation implementing part for detecting nodes of which the potential changes when a predetermined signal is applied to a logic circuit, as claim 1 requires; or the step of detection of nodes of which the potential changes when a predetermined signal is applied to a logic circuit, as recited in claim 6.

The Examiner relies upon col. 4 lines 18-24 for disclosing this feature. However, this portion of Ho discloses that the layout is a database containing the geometries and layers of the integrated circuit. Hence, Ho does not suggest detection of nodes of which the potential changes when a predetermined signal is applied to a logic circuit.

Further, Ho does not disclose extracting parasitic elements from the nodes of which the potential changes, as the claims 1 and 6 require. Instead, the reference discloses extracting layout parasitics for unspecified selected nodes or an entire circuit (col. 5, lines 48-50).

Accordingly, Ho does not expressly disclose the features discussed above.

In the event the Examiner relied upon inherency without expressly indicating such reliance, the Examiner should be aware that inherency requires certainty, not speculation. ***In re***

Rijckaert, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); ***In re King***, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986); ***W. L. Gore & Associates, Inc. v. Garlock, Inc.***, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); ***In re Oelrich***, 666 F.2d 578, 212 USPQ 323 (CCPA 1981); ***In re Wilding***, 535 F.2d 631, 190 USPQ 59 (CCPA 1976). To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. ***In re Robertson***, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). The Examiner provided no factual basis upon which to conclude that Ho discloses the claimed pre-layout simulation implementing part for detecting nodes of which the potential changes when a predetermined signal is applied to a logic circuit; and the parasitic element extraction part connected to the pre-layout simulation implementing part which extracts parasitic elements from the nodes of which the potential changes.

Moreover, it is respectfully submitted that Ho provides no reason for one skilled in the art to conclude that these features are necessarily present in the Ho system.

Accordingly, Ho neither expressly nor inherently discloses:

- a pre-layout simulation implementing part for detecting nodes of which the potential changes when a predetermined signal is applied to a logic circuit; and

- a parasitic element extraction part connected to the pre-layout simulation implementing part which extracts parasitic elements from the nodes of which the potential changes, as claim 1 requires, or

-the step of detection of nodes of which the potential changes when a predetermined signal is applied to a logic circuit; and

-the step of extracting parasitic elements from said nodes of which the potential changes, as claim 6 requires.

Accordingly, Ho does not describe the claimed invention within the meaning of 35 U.S.C. § 102. ***Kalman v. Kimberly-Clark Corp., supra***. Applicants, therefore, respectfully submit that the rejection of claims 1-10 under 35 U.S.C. § 102 as anticipated by Ho is untenable and should be withdrawn.

In view of the foregoing, and in summary, claims 1-10 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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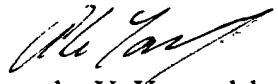

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IN THE DRAWINGS

Please replace FIGS. 8B, 9A, 9B, 10B and 11 with attached replacement sheets.